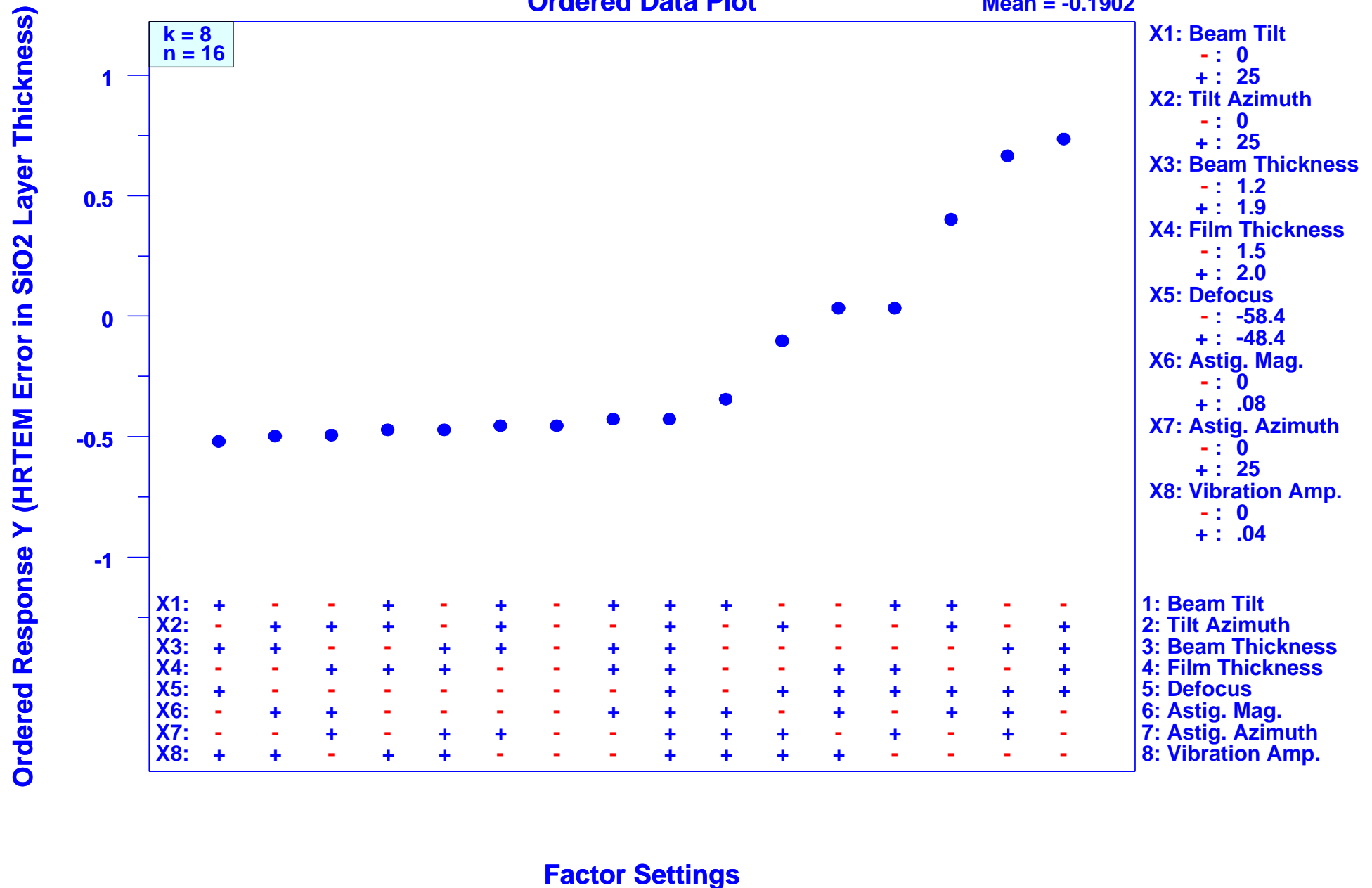
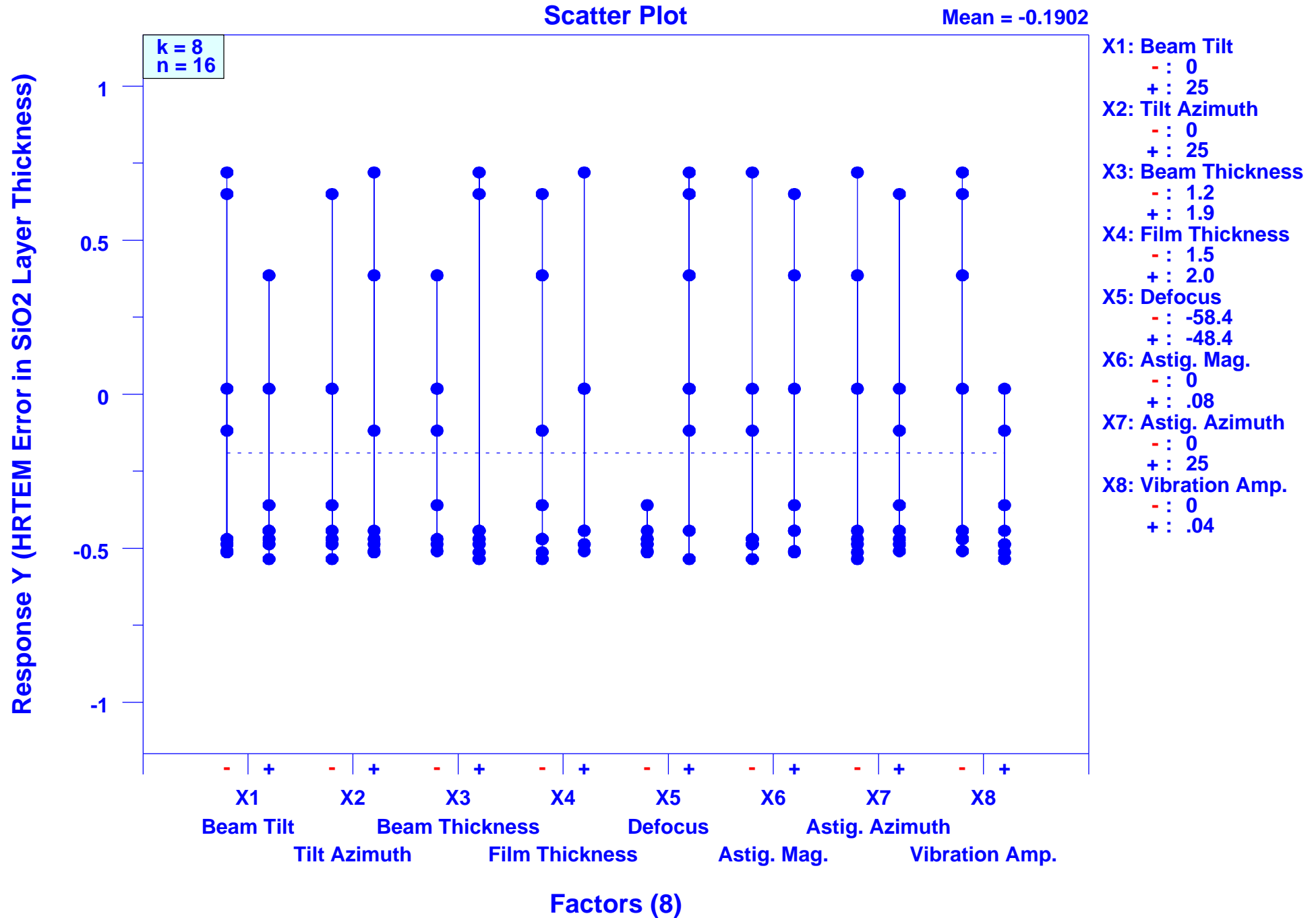
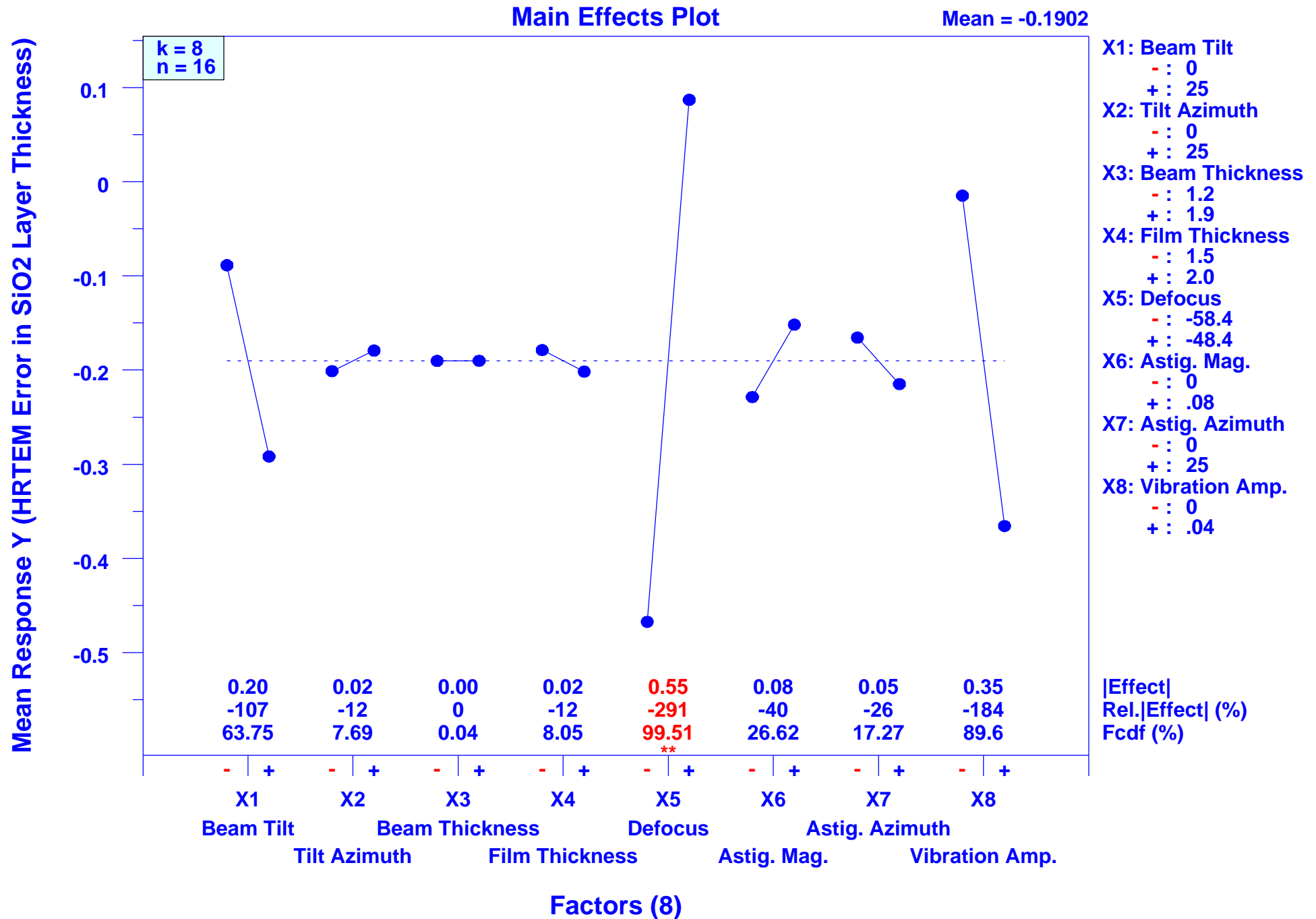


HRTEM Factors Affecting Thickness Measurements of Ultrathin Amorphous SiO₂ Layer in CPU/Memory Gate Dielectrics (Nanotechnology)

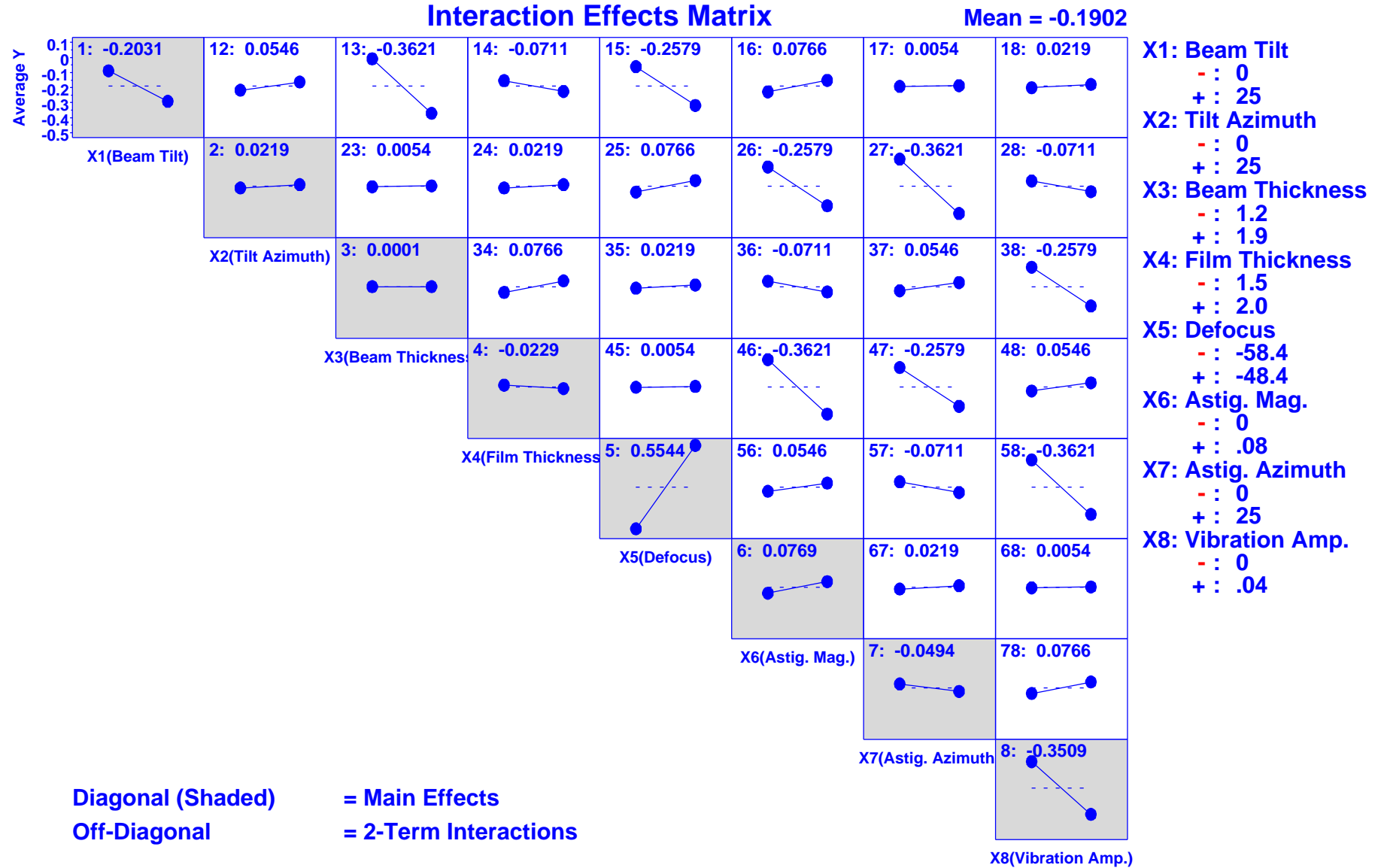


HRTEM Factors Affecting Thickness Measurements of Ultrathin Amorphous SiO₂ Layer in CPU/Memory Gate Dielectrics (Nanotechnology)



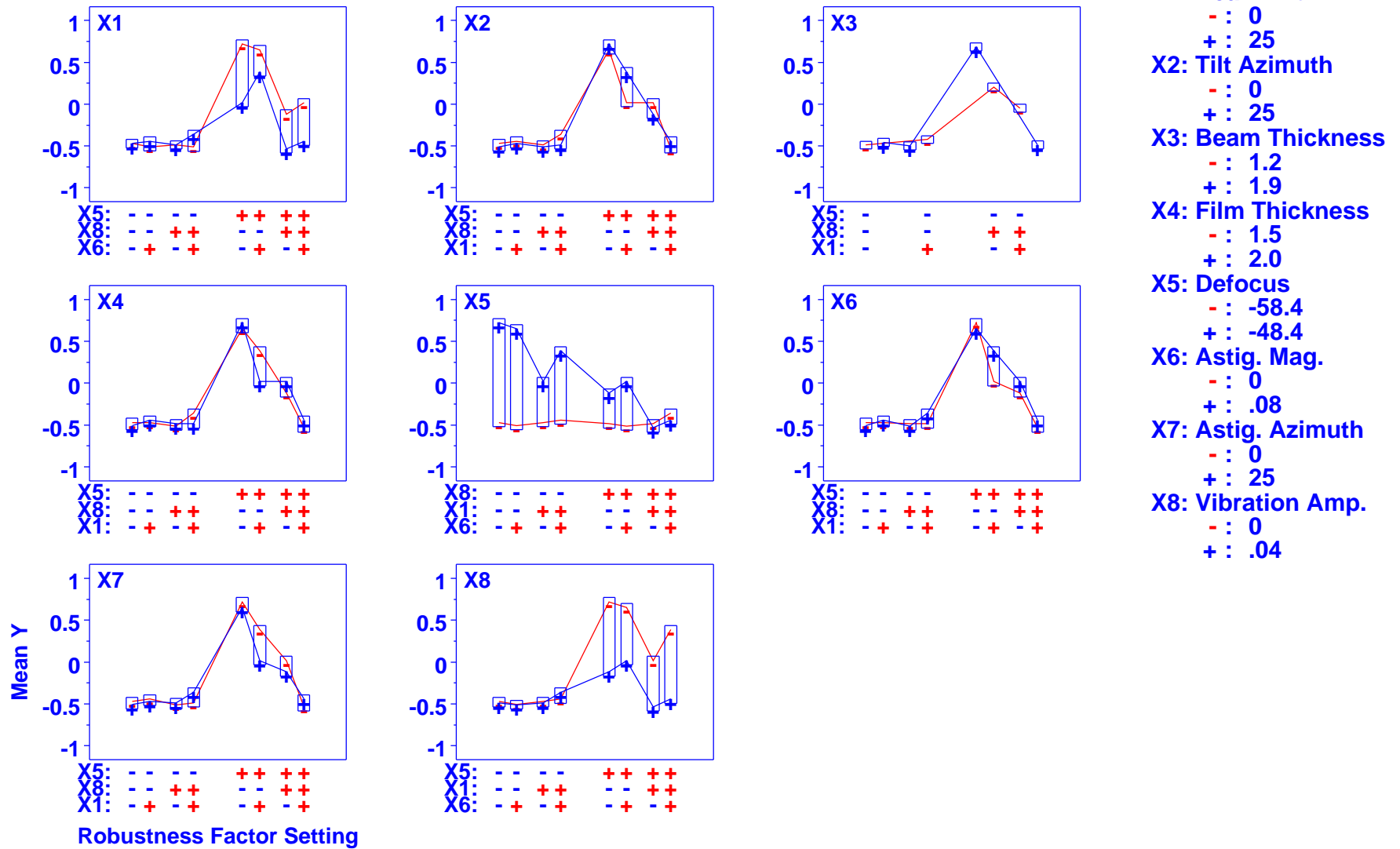


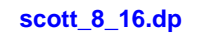
HRTEM Factors Affecting Thickness Measurements of Ultrathin Amorphous SiO₂ Layer in CPU/Memory Gate Dielectrics (Nanotechnology)



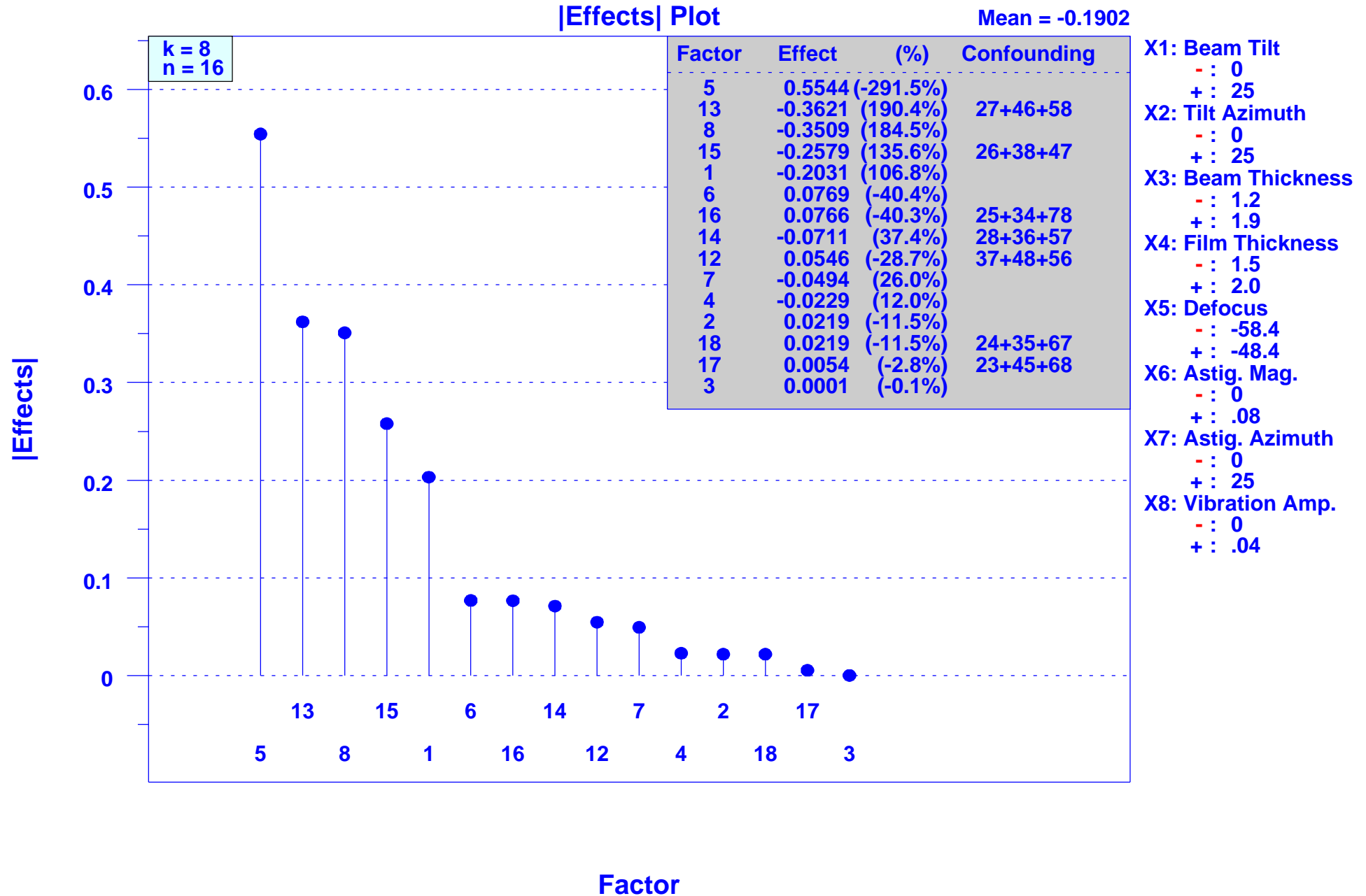
HRTEM Factors Affecting Thickness Measurements of Ultrathin Amorphous SiO₂ Layer in CPU/Memory Gate Dielectrics (Nanotechnology)

Block Plot

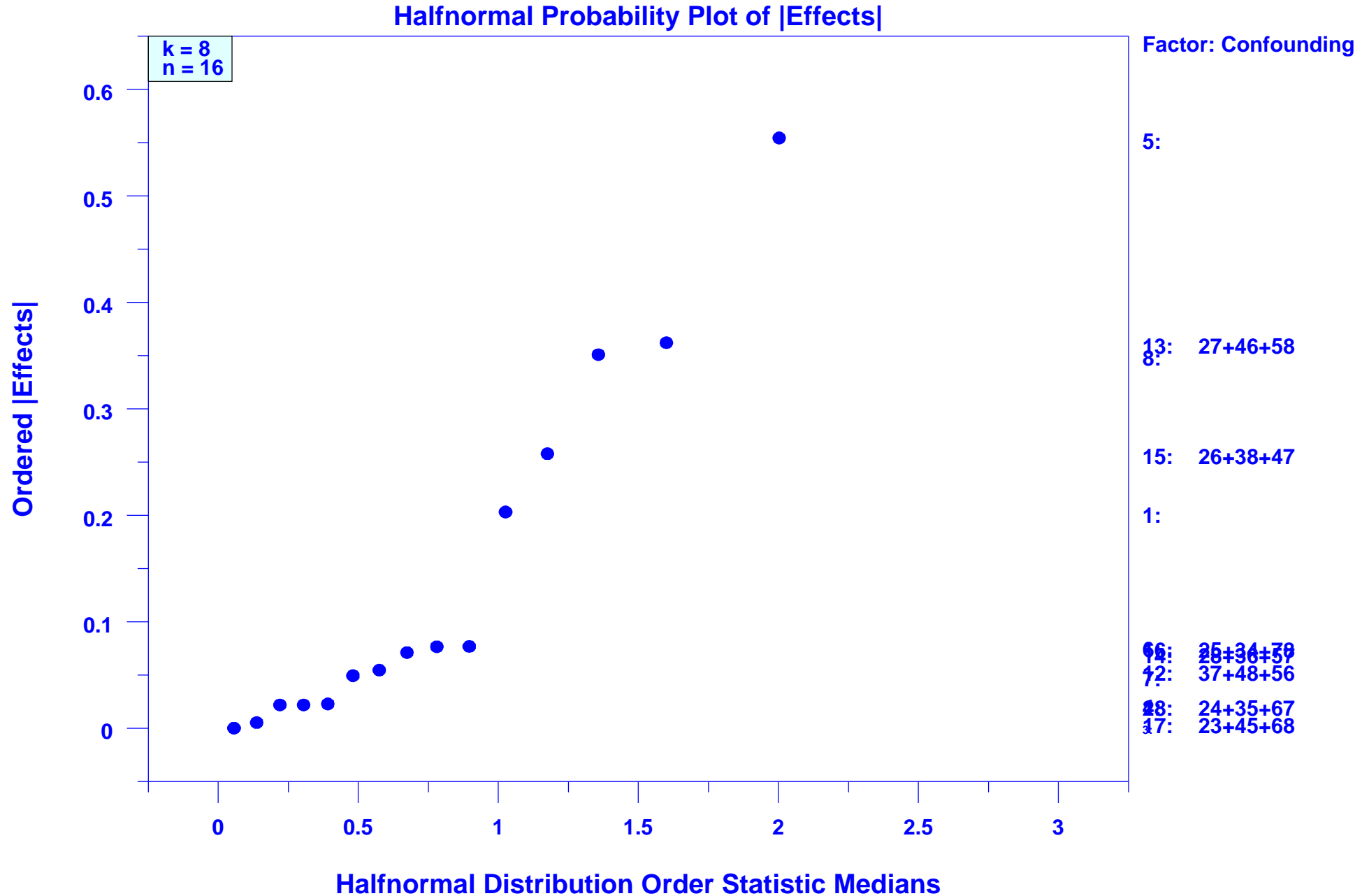




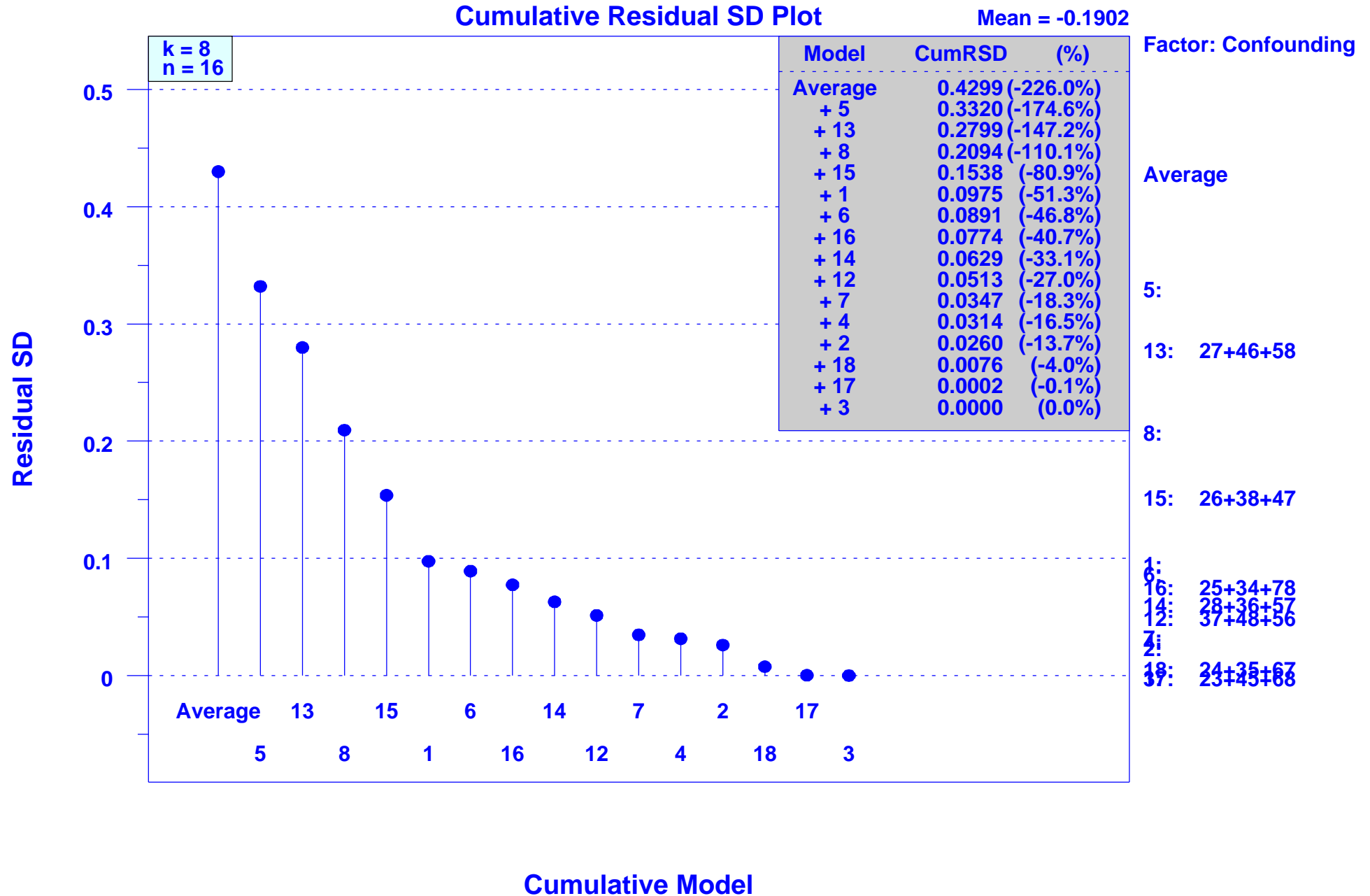
HRTEM Factors Affecting Thickness Measurements of Ultrathin Amorphous SiO₂ Layer in CPU/Memory Gate Dielectrics (Nanotechnology)



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Contour Plot of 2 Dominant Factors: X5 (Defocus) & X1 (Beam Tilt)

